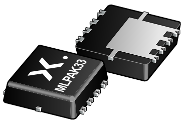


BUK6Q100-80P

80 V, P-channel Trench MOSFET

1 October 2025 — Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in an MLPAK33-WF (SOT8002-3) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Logic-level compatible
- Very fast switching
- Trench MOSFET technology
- Side-wettable flanks for optical solder inspection
- Thermally efficient package in a small form factor (3.3 mm x 3.3 mm footprint)
- AEC-Q101 qualified

3. Applications

- Reverse polarity protection
- High-speed line driver
- High-side load switch
- Relay driver

4. Quick reference data

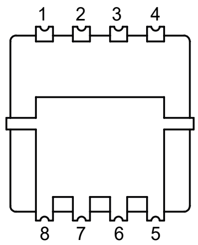
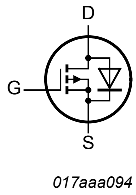
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	-80	V
V_{GS}	gate-source voltage	T_j = 25 °C	[1]	-20	-	20	V
I_D	drain current	V_{GS} = -10 V; T_{mb} = 25 °C		-	-	-16	A
P_{tot}	total power dissipation	T_{mb} = 25 °C		-	-	56	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = -10 V; I_D = -2.9 A; T_j = 25 °C		-	81	100	mΩ

[1] See application note AN90001.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 MLPAK33 (SOT8002-3)	
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK6Q100-80P	MLPAK33	plastic thermal enhanced surface mounted package with side-wettable flanks (SWF); mini leads; 8 terminals;pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-3

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK6Q100-80P	NXG

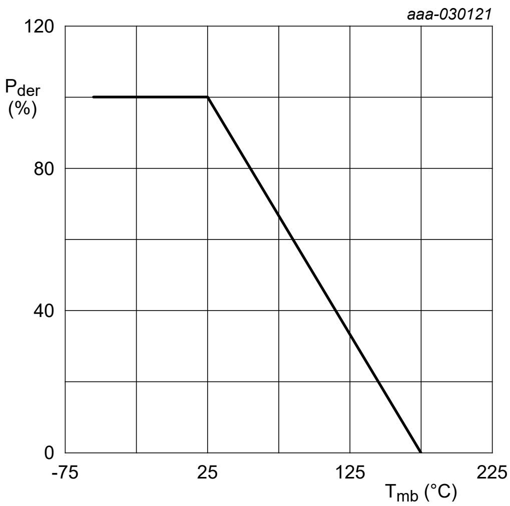
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

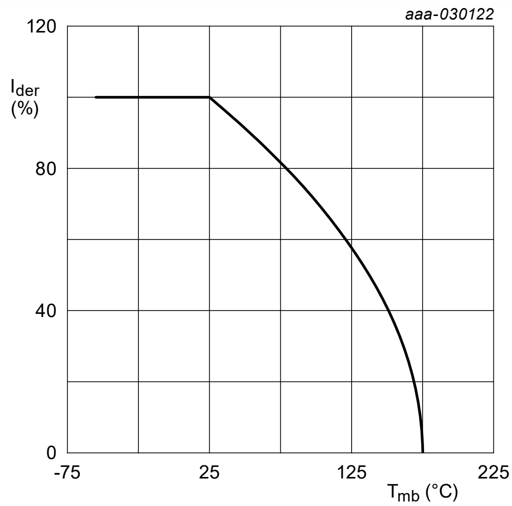
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-80	V
V_{GS}	gate-source voltage	T_j = 25 °C	[1]	-20	20	V
I_D	drain current	V_{GS} = -10 V; T_{mb} = 25 °C		-	-16	A
		V_{GS} = -10 V; T_{mb} = 100 °C		-	-11	A
I_{DM}	peak drain current	single pulse; t_p ≤ 10 µs; T_{mb} = 25 °C		-	-64	A
P_{tot}	total power dissipation	T_{mb} = 25 °C		-	56	W
T_j	junction temperature			-55	175	°C
T_{amb}	ambient temperature			-55	175	°C
T_{stg}	storage temperature			-65	175	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	-16	A
I_{SM}	peak source current	T_{mb} = 25 °C; single pulse; t_p ≤ 10 µs		-	-64	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{sup} ≤ -80 V; V_{GS} = -10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω; I_D = -22.8 A; unclamped	[2] [3]	-	49	mJ
I_{AS}	non-repetitive avalanche current	$T_{j(init)}$ = 25 °C	[4]	-	-22.8	A

[1] See application note AN90001.
[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
[3] Refer to application note AN10273 for further information.
[4] Protected by 100% test.



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\ \%$$

Fig. 2. Normalized continuous drain current as a function of mounting base temperature

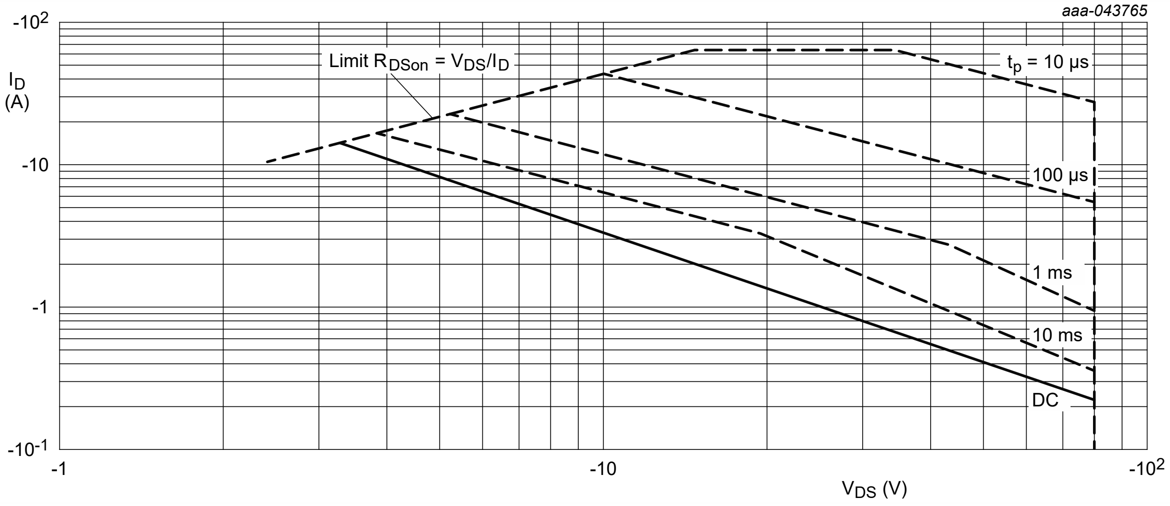


Fig. 3. Safe operating area; junction to mounting base; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	60	80	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base			-	1.8	2.7	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm^2.

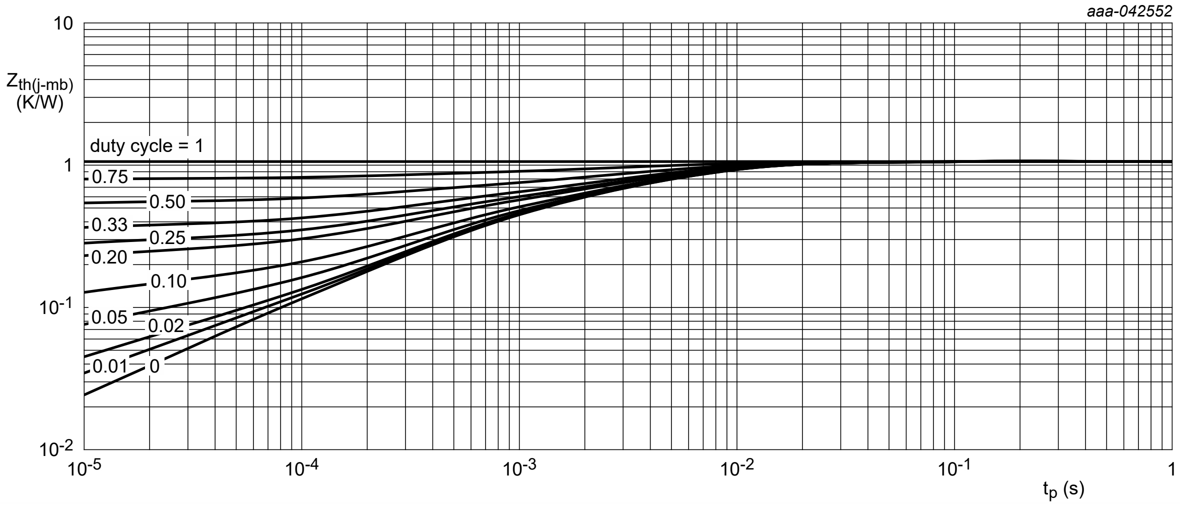


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = -250 µA; V_{GS} = 0 V; T_j = 25 °C		-80	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = -1 mA; V_{DS} = V_{GS}; T_j = 25 °C		-1.4	-2	-2.7	V
I_{DSS}	drain leakage current	V_{DS} = -80 V; V_{GS} = 0 V; T_j = 25 °C		-	-	-1	µA
		V_{DS} = -80 V; V_{GS} = 0 V; T_j = 125 °C		-	-	-20	µA
I_{GSS}	gate leakage current	V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	-	-100	nA
		V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = -10 V; I_D = -2.9 A; T_j = 25 °C		-	81	100	mΩ
		V_{GS} = -10 V; I_D = -2.9 A; T_j = 175 °C		-	180	230	mΩ
		V_{GS} = -4.5 V; I_D = -2.5 A; T_j = 25 °C		-	93	137	mΩ
g_{fs}	forward transconductance	V_{DS} = -5 V; I_D = -2.9 A; T_j = 25 °C		-	12.9	-	S
R_G	gate resistance	f = 1 MHz		-	11	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	V_{DS} = -40 V; I_D = -2.9 A; V_{GS} = -10 V; T_j = 25 °C		-	21.5	32	nC
Q_{GS}	gate-source charge			-	3.4	-	nC
Q_{GD}	gate-drain charge			-	5	-	nC
C_{iss}	input capacitance	V_{DS} = -40 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 °C		-	1090	-	pF
C_{oss}	output capacitance			-	72	-	pF
C_{rss}	reverse transfer capacitance			-	39	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = -40 V; I_D = -2.9 A; V_{GS} = -10 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	3	-	ns
t_r	rise time			-	5	-	ns
$t_{d(off)}$	turn-off delay time			-	41	-	ns
t_f	fall time			-	173	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = -1.9 A; V_{GS} = 0 V; T_j = 25 °C		-	-0.7	-1.2	V
t_{rr}	reverse recovery time	I_S = -1.9 A; dI_S/dt = 100 A/µs; V_{GS} = 0 V; V_{DS} = -40 V; T_j = 25 °C		-	25	-	ns
Q_r	recovered charge			-	27	-	nC

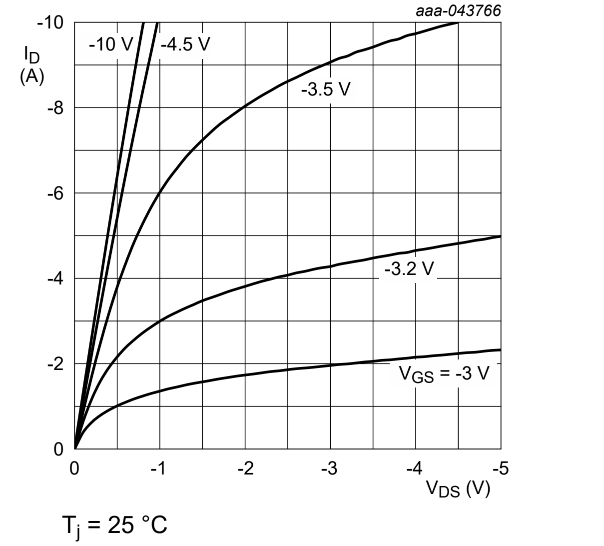


Fig. 5. **Output characteristics: drain current as a function of drain-source voltage; typical values**

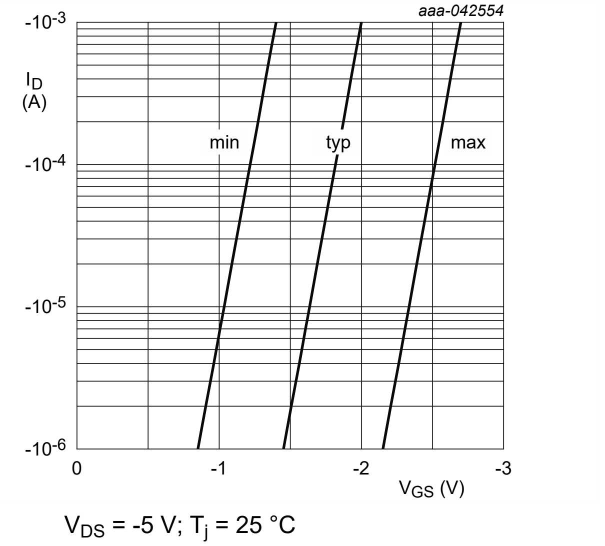


Fig. 6. **Sub-threshold drain current as a function of gate-source voltage**

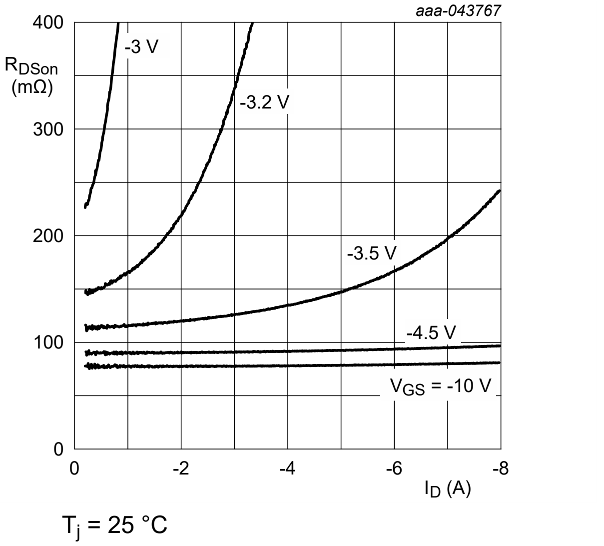


Fig. 7. **Drain-source on-state resistance as a function of drain current; typical values**

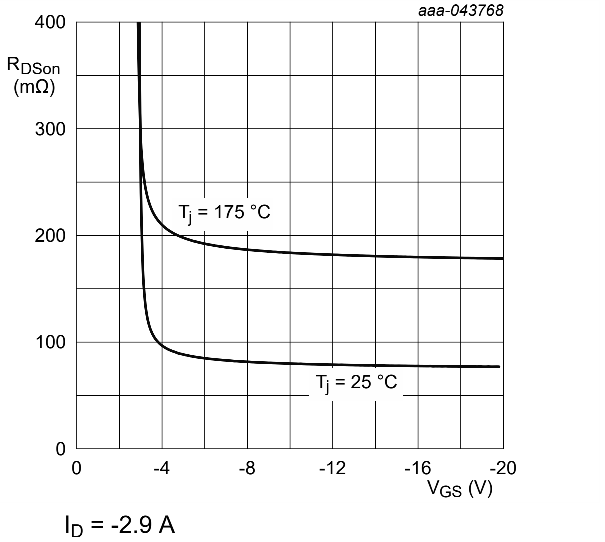
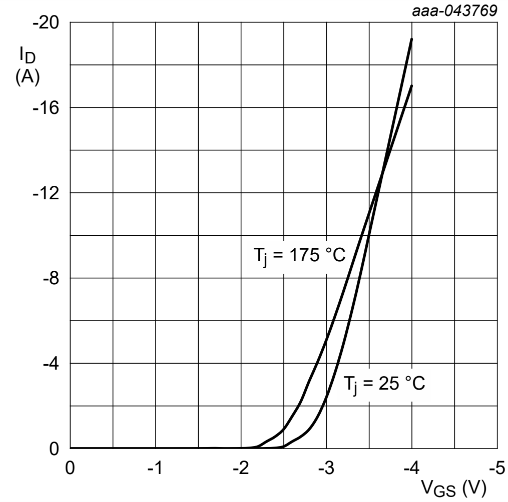
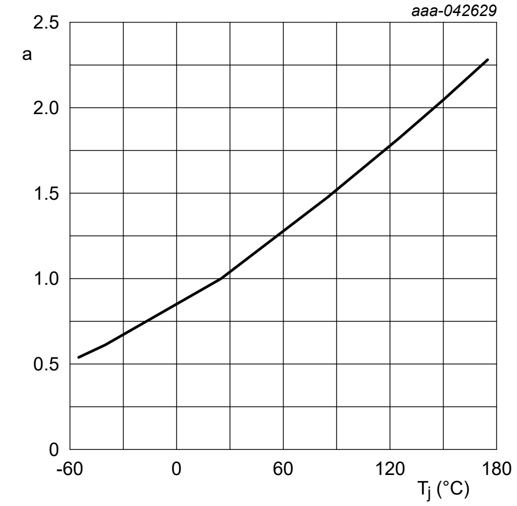


Fig. 8. **Drain-source on-state resistance as a function of gate-source voltage; typical values**



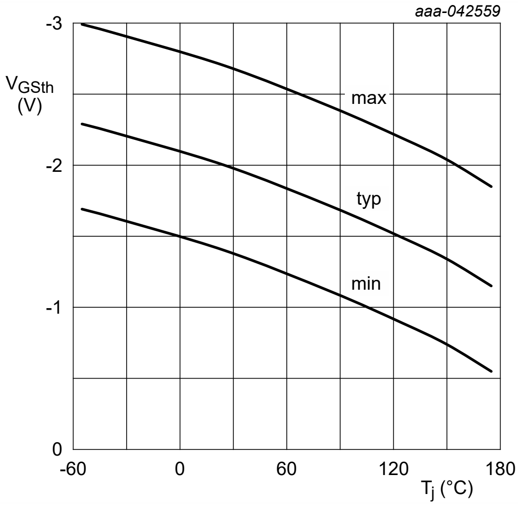
V_{DS} = -4 V

Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values



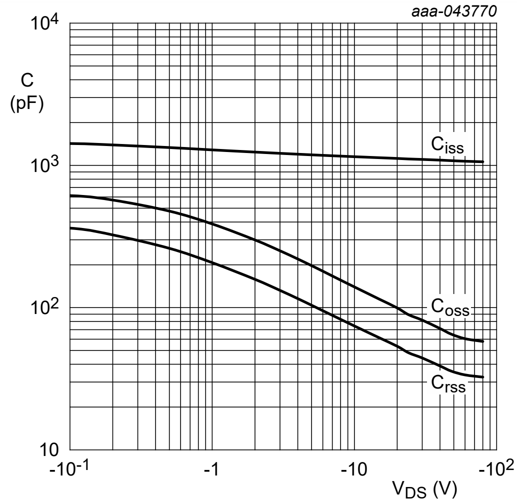
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig. 10. Normalized drain-source on-state resistance as a function of junction temperature; typical values



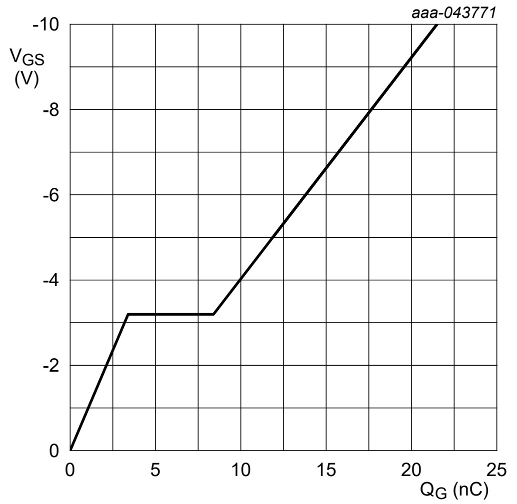
I_D = -1 mA; V_{DS} = V_{GS}

Fig. 11. Gate-source threshold voltage as a function of junction temperature



f = 1 MHz; V_{GS} = 0 V

Fig. 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



V_{DS} = -40 V; I_D = -2.9 A; T_j = 25 °C

Fig. 13. Gate-source voltage as a function of gate charge; typical values

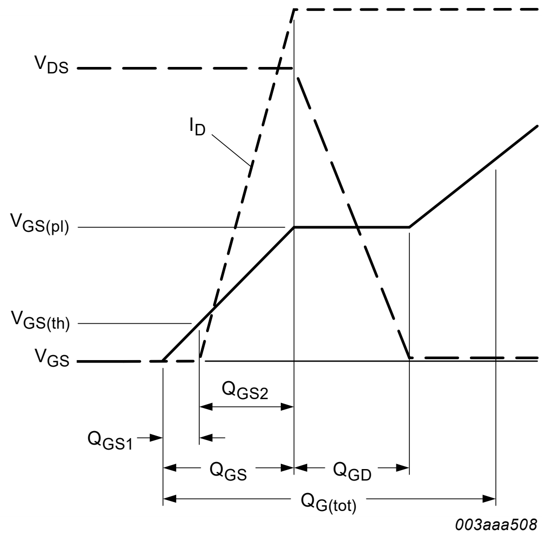
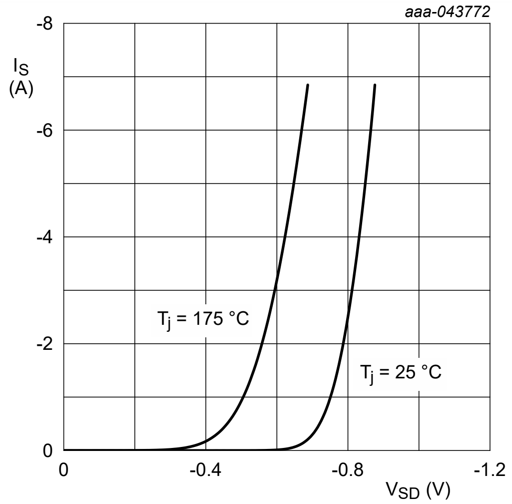


Fig. 14. Gate charge waveform definitions



V_{GS} = 0 V

Fig. 15. Source current as a function of source-drain voltage; typical values

11. Test information

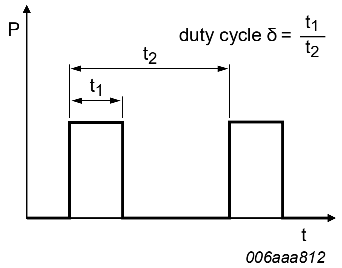


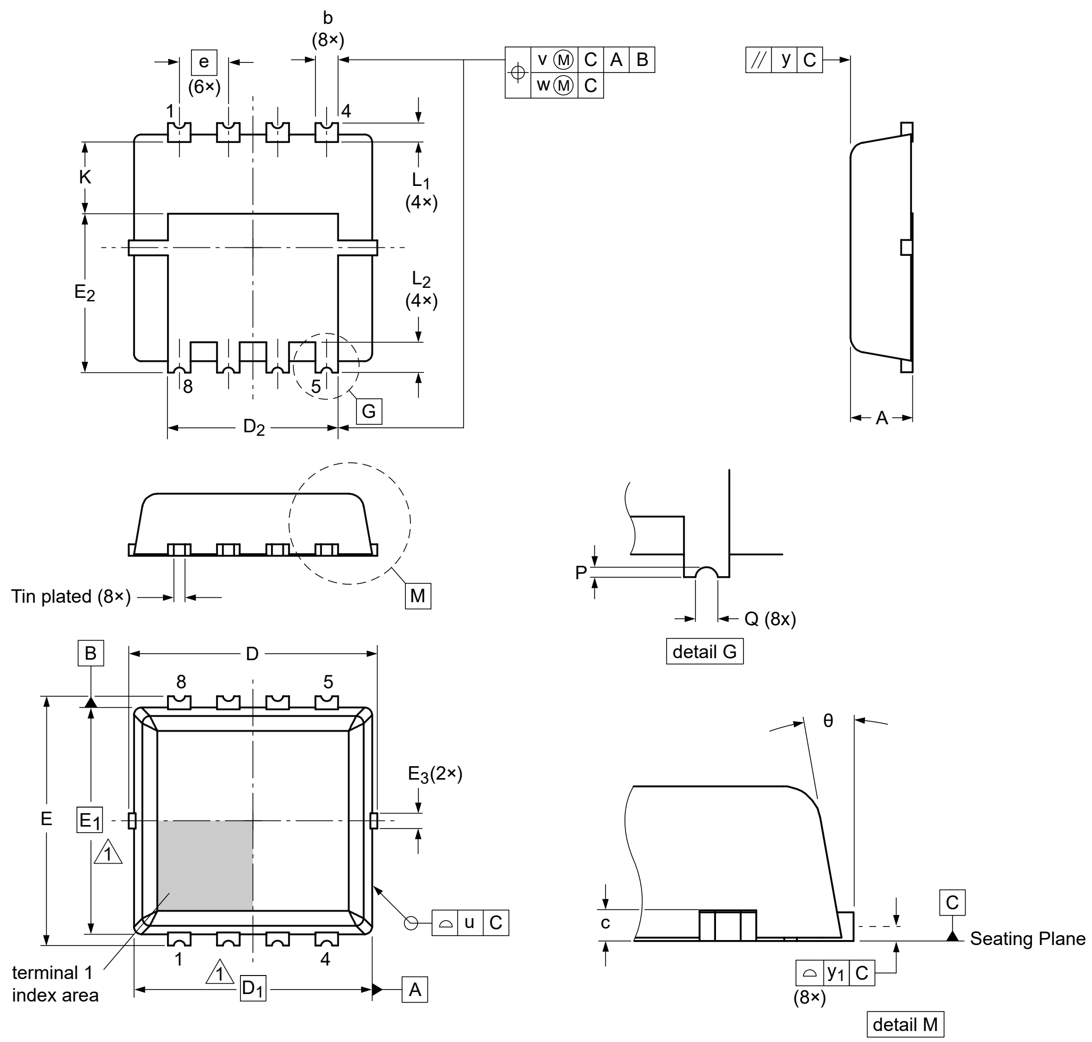
Fig. 16. Duty cycle definition

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

MLPAK33: plastic thermal enhanced surface mounted package with side-wettable flanks (SWF); mini leads; 8 terminals;pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body **SOT8002-3**



Dimensions do not include mold flash, protrusions of gate burrs, mold flash, tie bar protrusion or tie bar flash. Mold flash shall not be greater than 0.05 mm

Dimensions (mm are the original dimensions)

Unit		A	b	c	D	D_1	D_2	e	E	E_1	E_2	E_3	K	L_1	L_2	P	Q	θ	y	y_1	u	v	w
mm	max	0.90	0.40	0.18	3.40		2.35		3.40		2.20			0.40	0.55			12°					
	nom	0.80	0.32	0.15	3.30	3.15 BSC	2.25	0.65 BSC	3.30	3.0 BSC	2.10	0.2 REF	0.95 REF	0.25	0.40	0.1 REF	0.15 REF	10°	0.05	0.05	0.1	0.1	0.05
	min	0.70	0.25	0.12	3.20		2.15		3.20		2.00			0.10	0.25			8°					

sot8002-3_po

Outline version	References IEC	JEDEC	JEITA		European projection	Issue date
SOT8002-3						23-07-21

Fig. 17. Package outline MLPAK33 (SOT8002-3)

13. Soldering

Footprint information for reflow soldering of MLPAK33 package SOT8002-3

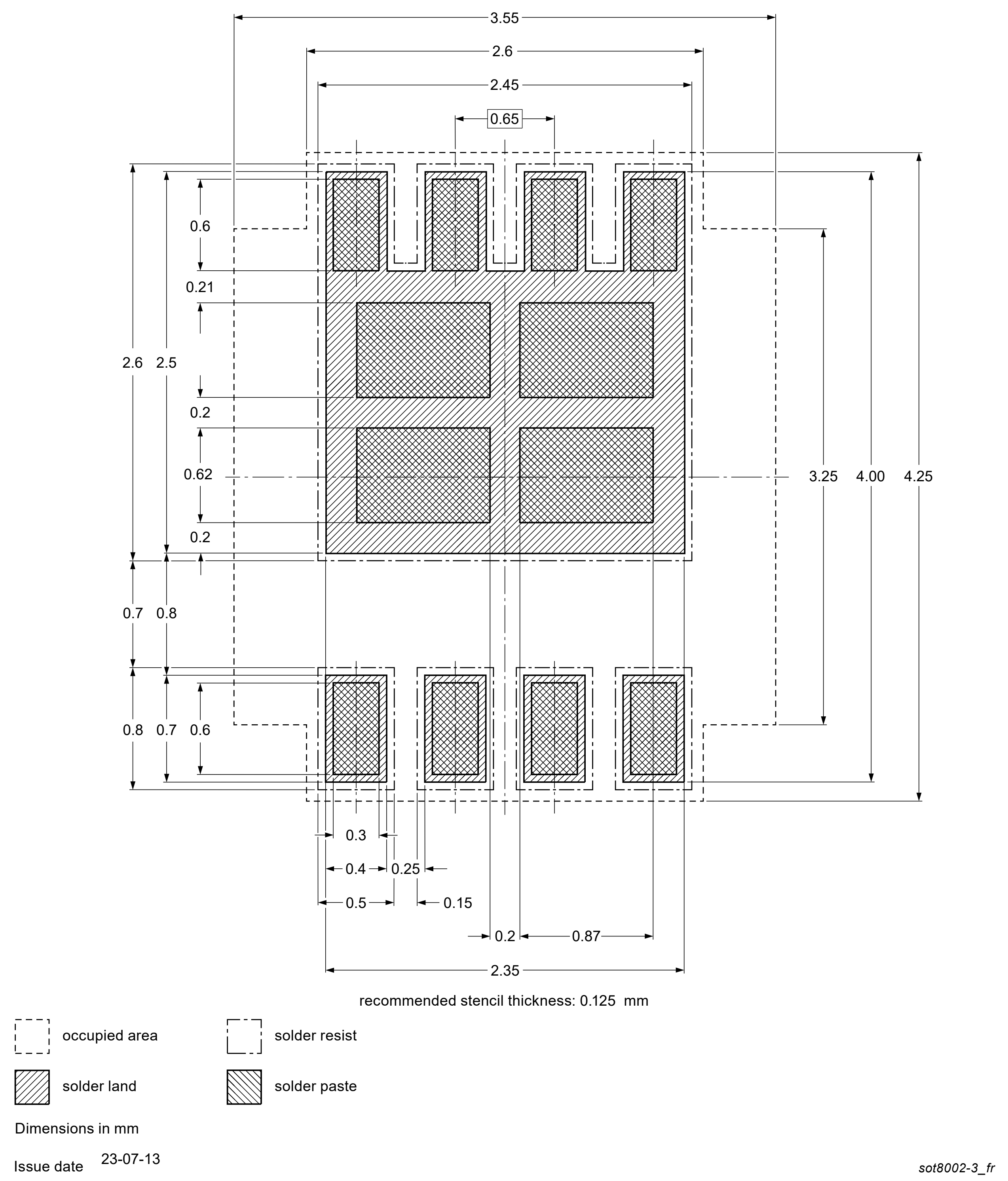


Fig. 18. Reflow soldering footprint for MLPAK33 (SOT8002-3)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
BUK6Q100-80P v.1	20251001	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 1 October 2025